CLAIMS

What is claimed is:

1. An electrostatic discharge protection device comprising:

a silicon controlled rectifier (SCR) constructed on a base region of a first conductivity type, the SCR including a well region of a second conductivity type formed in the base region, a first region of the first conductivity type formed in the well region, a second region of the second conductivity type formed in the well region, a third region of the first conductivity type formed in the base region, and a fourth region of the second conductivity type formed in the base region; and

an external pumping circuit comprising a transistor coupled to the well region or the base region, the transistor providing a pump current during an ESD event effective to lower the potential of the well region or the base region to which the transistor is coupled.

2. The electrostatic discharge device of claim 1, the transistor comprising a metal-oxide semiconductor field effect transistor (MOSFET).

3. The electrostatic discharge device of claim 1 further comprising a fifth region of the second conductivity type formed at the interface between the well region and the base region, the transistor being coupled to the well region through the fifth region.

4. The electrostatic discharge device of claim 3, the fifth region having a first width, and the transistor comprising a sixth region and a seventh region, the sixth region and the seventh region each having a second width greater than the first width.

5. The electrostatic discharge device of claim 4, the first region, the second region, the third region, and the fourth region, each having a third width, the third width being greater than the first width of the fifth region.

6. The electrostatic discharge device of claim 3, the first conductivity type being a p-type and the second conductivity type comprising an n-type.

7. The electrostatic discharge device of claim 3, the second region being coupled to a protected node and the third region being coupled to a grounded node.

8. The electrostatic discharge device of claim 7, the transistor comprising an nMOSFET with a drain, a source, and a gate, the drain being coupled to the fifth region, the source being coupled to the grounded node, and the gate being coupled to the protected node.

9. The electrostatic discharge device of claim 8, the external pumping circuit further comprising a capacitor and a resistor, the gate being coupled to the protected node through the capacitor, the gate being coupled to the source through the resistor.

10. The electrostatic discharge device of claim 9, the base region being a p-type substrate, the well region being an n-well, the first region and fourth region comprising p^+ type dopants, and the second region, the third region, and the fifth region comprising n^+ type dopants.

11. An electrostatic discharge protection device comprising:

a silicon controlled rectifier (SCR) constructed on a base region of a first conductivity type, the SCR including a well region of a second conductivity type formed in the base region, a first region of the first conductivity type formed in the well region, a second region of the second conductivity type formed in the well region, a third region of the first conductivity type formed in the base region, and a fourth region of the second conductivity type formed in the base region; each of the first, second, third, and fourth region having a first width, and

an external pumping circuit comprising a transistor coupled to the well region or to the base region, the transistor including a sixth region and a seventh region of the first conductivity type or the second conductivity type, the sixth region and the

seventh region having a second width substantially greater than the first width, the transistor providing a pump current to the SCR during an ESD event effective to lower the potential of the well region or the base region to which the transistor is coupled.

12. The electrostatic discharge device of claim 11, the transistor comprising a metal-oxide semi-conductor field effect transistor (MOSFET) or a bipolar junction transistor (BJT).

13. The electrostatic discharge device of claim 11, further comprising a fifth region of a second conductivity type formed at an interface between the well region and the base region, the transistor being coupled to the well region through the fifth region.

14. The electrostatic discharge device of claim 13, the fifth region having a third width substantially smaller the first width and the second width.

15. The electrostatic discharge device of claim 13, the first conductivity type being a p-type and the second conductivity type being an n-type.

16. The electrostatic discharge device of claim 13, the second region being coupled to a protected node and the third region being coupled to a grounded node.

17. The electrostatic discharge device of claim 16, the transistor comprising an nMOSFET having a drain, a source, and a gate, the drain being coupled to the fifth region, the source being coupled to the grounded node, and the gate being coupled to the protected node.

18. The electrostatic discharge device of claim 17, the external pumping circuit further comprising a capacitor and a resistor, the gate being coupled to the protected node through the capacitor, the gate being coupled to the source through the resistor.

19. The electrostatic discharge device of claim 18, the base region being a p-type substrate, the well region being an n-well, the first region and fourth region comprising p^+ type dopants, and the second region, the third region, the fifth region, the sixth region, and the seventh region comprising n^+ type dopants.

20. An electrostatic discharge protection device comprising:

a silicon controlled rectifier (SCR) constructed p-type substrate, the SCR including an n-well region formed in the p-type substrate with a first nmoat formed in the n-well region, a first pmoat formed in the n-well region, a second nmoat formed in the p-type substrate, a second pmoat formed in the p-type substrate, and a third nmoat formed at an interface between the n-well region and p-type substrate, the third nmoat having a first width; and

an external pumping circuit comprising an nMOSFET, the nMOSFET including a source, a drain, and a gate, the drain being coupled to the third nmoat, the source and drain each having a width effective to provide a pump current during an ESD event to the third nmoat to lower the potential of the nwell region.

21. The electrostatic discharge device of claim 20, the first pmoat being coupled to a protected node and the second nmoat being coupled to a grounded node.

22. The electrostatic discharge device of claim 20, the external pumping circuit further comprising a capacitor and a resistor, the gate being coupled to the protected node through the capacitor, the gate being coupled to the source through the resistor.

23. The electrostatic discharge device of claim 20, the ratio of the second width to the first width being at lease about three to one.

24. The electrostatic discharge device of claim 23, the ratio of the second width to the first width being at least about twelve to one.